WHAT IS CLAIMED IS:

1. A clock/data recovery circuit comprising:

a voltage control oscillator for generating a clock signal of a frequency of 1/K (K=2,3,···) of a bit rate of an input data signal;

a delay circuit for delaying said input data signal for timing adjustment;

a demultiplexer for demultiplexing said input data signal into M demultiplexed signals (M=2,3,···) by using said clock signal;

a multiplexer for multiplexing said M demultiplexed signals by using said clock signal;

a phase comparator for comparing phases of an output signal of said delay circuit and an output signal of said multiplexer;

a lowpass filter for extracting DC voltage from an output signal of said phase comparator and for inputting said DC voltage to said voltage control oscillator as a control voltage;

wherein said clock/data recovery circuit outputs said clock signal generated by said voltage control oscillator as a recovery divided clock signal, and outputs said M demultiplexed signals from said demultiplexer as recovery parallel data signals.

2. The clock/data recovery circuit as claimed in claim 1, wherein $M=K\times L$ in which L is a natural number.

3. The clock/data recovery circuit as claimed in claim 1, said clock/data recovery circuit comprising:

another delay circuit, provided before said delay circuit, for delaying said input data signal; and

another phase comparator, instead of said phase comparator, for comparing phases of said output signal of said delay circuit and said output signal of said multiplexer, and comparing phases of a result of comparison of phases of said output signal of said delay circuit and said output signal of said multiplexer and an output signal of said another delay circuit.

4. The clock/data recovery circuit as claimed in claim 1, when K=2 and M=2, said demultiplexer comprising:

a first D-type ms-flip flop circuit for receiving said input data signal by using said clock signal; and

a second D-type ms-flip flop circuit for receiving said input data signal by using an inverted signal of said clock signal;

said multiplexer comprising:

a clock delay circuit for delaying said clock signal; and

a selector for selecting alternately an output signal of said first D-type ms-flip flop circuit and an output signal of said second D-type ms-flip flop circuit by using an output signal of said clock delay circuit.

5. The clock/data recovery circuit as claimed in claim 2, when K=2, said demultiplexer comprising:

a first demultiplexer for demultiplexing said input data signal into two first parallel data signals by using said clock signal;

two second demultiplexers each of which demultiplexes one of said first parallel signals into L second parallel data signals by using a divided clock signal generated dividing said clock signal by L and said clock signal;

said multiplexer comprising:

two first multiplexers each of which multiplexes said L second parallel data signals into serial data by using said divided clock signal and said clock signal; and

a second multiplexer for multiplexing two parallel data signals output from said two first multiplexer into serial data by using said clock signal.

6. The clock/data recovery circuit as claimed in claim 2, when K=2 and $M=2^T$ (T is an integer equal to or larger than 2), said demultiplexer comprising:

T stages in which a Qth (Q=1,2,3$\cdots$T) stage includes $2^{(Q-1)}$ 1:2 demultiplexers, and a divided clock signal generated by dividing said clock signal by $2^{(Q-1)}$ is provided to each 1:2 demultiplexer in said Qth stage;

said multiplexer comprising:

T stages in which a Qth (Q=1,2,3···T) stage includes $2^{(T-Q)}$ 2:1 multiplexers, a divided clock signal generated by dividing said clock signal by $2^{(T-Q)}$ is provided to each 2:1 multiplexer.

7. The clock/data recovery circuit as claimed in claim 2, when K>2, said demultiplexer comprising:

a part for generating K-1 signals in which phases are different each other with respect to said clock signal;

a first demultiplexer for demultiplexing said input data signal into K first parallel data signals by using said K-1 signals and said clock signal; and

K second demultiplexers each of which demultiplexes one of said first parallel data signals into L second parallel data signals;

said multiplexer comprising:

K first multiplexer each of which multiplexes said L second parallel data signals into serial data by using said divided clock signal and said clock signal; and

a second multiplexer for multiplexing K parallel data signals output from said K first multiplexers into serial data by using a multiplied signal generated by multiplying said clock signal and said clock signal.

8. A clock/data recovery circuit comprising:

a voltage control oscillator for generating a clock signal of a frequency of 1/K (K=2,3,···) of a bit rate of an input data signal;

a Q divider for receiving said input data signal and for dividing a frequency of said input data signal by Q (Q=2,3,4···);

a first demultiplexer for demultiplexing an output signal of said Q divider into M demultiplexed signals (M=2,3,···) by using said clock signal;

a second demultiplexer for demultiplexing said input data signal into N demultiplexed signals by using said clock signal;

a multiplexer for multiplexing said M demultiplexed signals output from said first demultiplexer into a signal by using said clock signal;

a phase comparator for comparing phases of an output signal of said Q divider and an output signal of said multiplexer;

a lowpass filter for extracting DC voltage from an output signal of said phase comparator and for inputting said DC voltage to said voltage control oscillator as a control voltage; and

an m (=N/K) divider for dividing a frequency of an output clock signal of said voltage control oscillator by m;

wherein said clock/data recovery circuit outputs an output signal of said m (=N/K) divider as a recovery divided signal, and outputs said N demultiplexed signals output from said second demultiplexer as recovery parallel data signals.

9. The clock/data recovery circuit as

claimed in claim 8, wherein M=K×L in which L is a natural number.

10. The clock/data recovery circuit as claimed in claim 8, said clock/data recovery circuit comprising:

a delay circuit provided after said Q divider (Q=2,3,4···); and

another phase comparator, instead of said phase comparator, for comparing phases of an output signal of said delay circuit and said output signal of said multiplexer, and comparing phases of a result of comparison of phases of said output signal of said delay circuit and said output signal of said multiplexer and an output signal of said Q divider.

11. The clock/data recovery circuit as claimed in claim 8, when K=2 and M=2, said first demultiplexer comprising:

a first D-type ms-flip flop circuit for receiving an output signal of said Q divider by using said clock signal; and

a second D-type ms-flip flop circuit for receiving an output signal of said Q divider by using an inverted signal of said clock signal;

said multiplexer comprising:

a clock delay circuit for delaying said clock signal; and

a selector for selecting alternately an output signal of said first D-type ms-flip flop circuit and an output signal of said second D-type

ms-flip flop circuit by using an output signal of said clock delay circuit.

12. The clock/data recovery circuit as claimed in claim 1, when K=2, said clock/data recovery circuit comprising:

an m (=M/K) divider for outputting a divided clock signal generated by dividing said clock signal by m;

a 90-degree delay circuit for delaying said clock signal output from said voltage control oscillator by 90 degree; and

a multiplier for multiplying an output signal from said 90-degree delay circuit and a clock signal output from said voltage control oscillator, and outputting a clock signal the frequency of which is the same as bit rate of said input data signal;

wherein said clock/data recovery circuit outputs a data signal from said multiplexer and a clock signal from said multiplier as a serial data signal.

13. The clock/data recovery circuit as claimed in claim 3, when K=2, said clock/data recovery circuit comprising:

an m(=M/K) divider for outputting a divided clock signal generated by dividing said clock signal by m;

a 90-degree delay circuit for delaying said clock signal output from said voltage control oscillator by 90 degree; and

a multiplier for multiplying an output signal from said 90-degree delay circuit and a delay clock signal from said voltage control oscillator, and outputting a clock signal of which the frequency is the same as bit rate of said input data signal;

wherein said clock/data recovery circuit outputs a data signal from said multiplexer and a clock signal from said multiplier as a serial data signal.

14. The clock/data recovery circuit as claimed in claim 12, instead of providing said 90-degree delay circuit, wherein said voltage control oscillator outputs a quadrature clock signal having the same frequency as said clock signal and being quadrature to said clock signal, said multiplier receives said clock signal and said quadrature clock signal and outputs a clock signal having the same frequency as bit rate of said input data signal.

15. The clock/data recovery circuit as claimed in claim 1, said clock/data recovery circuit comprising:

an m divider for outputting a divided clock signal generated by dividing said clock signal by m; and

a K multiplier for multiplying said clock signal by K, so that a clock signal having the same frequency as bit rate of said input data signal is output;

wherein said clock/data recovery circuit

outputs a data signal from said multiplexer and a clock signal from said K multiplier as a serial data signal.

16. The clock/data recovery circuit as claimed in claim 14, said voltage control oscillator comprising 2k ($k \geqq 1$) buffer circuits having the same delay time in which said delay time is controlled by a control voltage, said buffer circuits being connected in series, an inverted signal of the output of a 2kth buffer circuit is input to a first stage buffer circuit;

wherein an input of said first stage buffer circuit is said clock signal and an output of kth stage buffer circuit is said quadrature clock signal.

17. The clock/data recovery circuit as claimed in claim 15, said K multiplier comprising:

a first phase comparator,

a lowpass filter for extracting DC voltage from an output signal of said first phase comparator;

a first voltage control oscillator in which the oscillation frequency is controlled by an output signal of said first lowpass filter; and

a K divider for dividing an output signal of said first voltage control oscillator by K

wherein said first phase comparator receives an output signal of said K divider and said clock signal of said voltage control oscillator, and

said first voltage control oscillator outputs a clock signal having the same frequency as bit rate of said input data signal.

18. A receiving apparatus including a clock/data recovery circuit, said clock/data recovery circuit comprising:

a voltage control oscillator for generating a clock signal of a frequency of 1/K (K=2,3,···) of a bit rate of an input data signal;

a delay circuit for delaying said input data signal for timing adjustment;

a demultiplexer for demultiplexing said input data signal into M demultiplexed signals (M=2,3,···) by using said clock signal;

a multiplexer for multiplexing said M demultiplexed signals by using said clock signal;

a phase comparator for comparing phases of an output signal of said delay circuit and an output signal of said multiplexer;

a lowpass filter for extracting DC voltage from an output signal of said phase comparator and inputting said DC voltage to said voltage control oscillator as a control voltage;

wherein said clock/data recovery circuit outputs said clock signal generated by said voltage control oscillator as a recovery divided clock signal, and outputs said M demultiplexed signals output from said demultiplexer as recovery parallel data signals.